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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,447	WILFRIED HAENSCH	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *33 and 34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with traverse of Species I, claims 1-32 which was filed on 7/7/05 is acknowledged. The traversal is on the ground(s) that there is not burden. This is not found persuasive because the inventions are classified in different classes and there are divergent subject matters and the search for a method for forming a CMOS well structure in species I is not required the same search in species II.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.

2. Claims 1-2, 26-27, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Masuoka et al. (U.S. 6,342,413).

As to claim 1, Masuoka et al. disclose method of forming a CMOS well structure, comprising: forming a first mask ("resist film 115" as mask) on a substrate 111, the first mask 115 having a plurality of openings; forming a plurality of first conductivity type wells ("p type well 116) over the substrate 111, each of the plurality of first conductivity type wells ("p type well 116") formed in a respective opening in the first mask 115; forming a cap over each of the first conductivity type wells; removing the first mask 115; forming sidewall spacers (343A, 343B, 343C, 343D, 343E, 343F) on sidewalls of each of the first conductivity type wells ("p type well 116"); and forming a plurality of second conductivity type wells, each of the plurality of

second conductivity type wells being formed between respective first conductivity type wells ("p type well 116") (see figures 2A-2C; 3I-3J; column 5, lines 49-57).

As to claim 2, Masuoka et al. disclose a plurality of shallow trench isolations ("element isolating regions 112") between the first conductivity type wells and second conductive type wells (p-type well 116); forming at least one second conductivity type MOS device (nMOS 113 or pMOS 114) inside each of the plurality of first conductivity type wells (p-type well 116); and forming at least one first conductivity type MOS device (nMOS 113 or pMOS 116) inside each of the plurality of second conductivity type wells (p-type well 116) (see figure 2A; column 5, lines 37-43; column 7, lines 63-67; column 8, lines 1-12).

As to claim 26, Masuoka et al. disclose method of forming a CMOS well structure, comprising: forming a first mask ("resist film 115" as mask) on a substrate 111, the first mask 115 having a plurality of openings; forming a plurality of first conductivity type wells ("p type well 116) over the substrate 111, each of the plurality of first conductivity type wells ("p type well 116") formed in a respective opening in the first mask 115; forming a cap over each of the first conductivity type wells; removing the first mask 115; forming sidewall spacers (343A, 343B, 343C, 343D, 343E, 343F) on sidewalls of each of the first conductivity type wells ("p type well 116"); and forming a plurality of second conductivity type wells, each of the plurality of second conductivity type wells being formed between respective first conductivity type wells ("p type well 116") (see figures 2A-2C; 3I-3J; column 5, lines 49-57).

As to claim 27, Masuoka et al. disclose a plurality of shallow trench isolations ("element isolating regions 112") between the first conductivity type wells and second conductive type wells (p-type well 116); forming at least one second conductivity type MOS device (nMOS 113

or pMOS 114) inside each of the plurality of first conductivity type wells (p-type well 116); and forming at least one first conductivity type MOS device (nMOS 113 or pMOS 116) inside each of the plurality of second conductivity type wells (p-type well 116) (see figure 2A; column 5, lines 37-43; column 7, lines 63-67; column 8, lines 1-12).

As to claim 32, Masuoka et al. disclose the first conductivity type is n-type (n-type wells 326-327) and the second conductivity type is p-type ("p type wells 324-325") (see figures 2A-2B; column 9, lines 16-47; figure 4D).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6, 9, 11, 15, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) in view of Hahn (US 6,482,717).

As to claim 3, Masuoka et al. do not disclose the plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process. Hahn (US 6,482,717) discloses the plurality of first conductivity type wells (wells 6) are formed by a first selective epitaxial growth process ("selective epitaxial growth SEG"), and the plurality of second conductivity type wells (wells 6) are formed by a second selective epitaxial growth process (see abstract; figures 1D-1G; column 2, lines 60-67; column 4, lines 23-37). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to

include a selective epitaxial growth process in Masuoka et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

As to claim 6, Masuoka et al. do not disclose a step of forming a plurality of first conductivity type wells comprises forming a first epitaxial layer in-situ doped with a first conductivity dopant. Hahn discloses a step of forming a plurality of first conductivity type wells (well 6) comprises forming a first epitaxial layer in-situ doped (doped in-situ) with a first conductivity dopant (see figures 1D-1G; column 4, lines 34-38). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include a selective epitaxial growth process in Masuoka et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

As to claim 9, Masuoka et al. do not disclose a step of forming a plurality of second conductivity type wells comprises forming a second epitaxial layer in-situ doped with a second conductivity dopant. Hahn discloses a step of forming a plurality of second conductivity type wells (well 6) comprises forming a second epitaxial layer in-situ doped (doped in-situ) with a second conductivity dopant (see figures 1D-1G; column 3, lines 13-17). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include a selective epitaxial growth process in Masuoka et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

As to claim 11, Masuoka et al. do not disclose a step of forming the second epitaxial layer to a larger thickness than that of the first conductivity type wells to avoid corner faceting; and planarizing the second epitaxial layer.

Hahn discloses a step of forming the second epitaxial layer ("oxide layer 5") to a larger thickness than that of the first conductivity type wells (wells 6) to avoid corner faceting; and planarizing the second epitaxial layer (planarization using Chemical Mechanical Polishing-CMP) (see column 4, lines 56-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include a selective epitaxial growth process and planarization process in Masuoka et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region and a semiconductor device with a flat surface.

As to claim 28, Masuoka et al. do not disclose the plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process. Hahn (US 6,482,717) discloses the plurality of first conductivity type wells (wells 6) are formed by a first selective epitaxial growth process ("selective epitaxial growth SEG"); and the plurality of second conductivity type wells (wells 6) are formed by a second selective epitaxial growth process (see abstract; column 2, lines 60-67; column 4, lines 23-37). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to selective epitaxial growth process in Masuoka et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

5. Claims 4-5, 12-18, 20, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) in view of Rengarajan et al. (U.S. 6,323,103).

As to claim 4, Masuoka et al. (U.S. 6,342,413) does not disclose: the first mask is a low-temperature chemical vapor deposition nitride.

Rengarajan et al. (U.S. 6,323,103) discloses the first mask ("masking layer 16") is a low-temperature chemical vapor deposition (low pressure chemical vapor deposition) nitride (silicon nitride Si3N4) (see column 5, lines 53-57). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use CVD for making a nitride layer in Masuoka et al. by providing CVD chemical vapor deposition as taught by Rengarajan et al. for the purpose of providing a better masking layer (see column 5, lines 53-57).

As to claim 5, Masuoka et al. (U.S. 6,342,413) does not disclose: the thickness of the first mask is in the range of about 50 nm to about 500 nm. Rengarajan et al. (U.S. 6,323,103) discloses the thickness of the first mask is in the range of about 50 nm to about 500 nm ("thickness of approximately 2,000 Angstroms") (see column 5, lines 53-57). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use CVD for making a nitride layer in Masuoka et al. by providing CVD chemical vapor deposition as taught by Rengarajan et al. for the purpose of providing a better masking layer with a precise and controlled thickness (see column 5, lines 53-57).

As to claim 12, Masuoka et al. do not teach: wherein step of forming a cap comprises thermal oxidation. Rengarajan et al. discloses: wherein step of forming a cap comprises thermal oxidation (forming dielectric caps 40A-40B) (see figures 2C-2F; column 8, lines 55-65). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to form a cap in Masuoka et al. as taught by Rengarajan et al. for the purpose of protecting gate electrodes (see figures 2C-2F; column 8, lines 55-65).

As to claim 13, Masuoka et al. disclose of forming sidewall spacers comprises chemical vapor deposition (side wall insulating film 135C are formed on side surfaces of the gate

electrode 134C and the gate insulating film 133C) (see figures 2D, 3I-3J; column 6, line 67; column 7, lines 1-2).

As to claim 14, Masuoka et al. do not disclose the sidewall spacers are made of nitride.

Rengarajan et al. disclose the sidewall spacers are made of nitride ("silicon nitride spacers 53") (see figure 2E; column 9, lines 38-41). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to form a nitride spacers in Masuoka et al. as taught by Rengarajan et al. for the purpose of insulating gate electrodes from any borderless contacts (see figure 2E; column 9, lines 38-41).

As to claim 15, Masuoka et al. do not disclose the thickness of the sidewalls spacers is in the range of about 5 nm to about 30 nm.

Rengarajan et al. disclose the thickness of the sidewalls spacers ("spacers 53") is in the range of about 5 nm to about 30 nm (see figure 2E)

As to claim 16, Masuoka et al. disclose the first conductivity type is n-type (n-type wells 326-327) and the second conductivity type is p-type ("p type wells 324-325") (see figures 2A-2B; column 9, lines 16-47; figure 4D).

As to claim 17, Masuoka et al. do not etching the substrate between the plurality of openings in the first mask to a predetermined depth before forming a plurality of first conductivity type wells over the substrate. Rengarajan et al. disclose etching (photolithographic-etching techniques) the substrate between the plurality of openings in the first mask ("masking layer 16") to a predetermined depth before forming a plurality of first conductivity type wells (openings 18 for forming active area) over the substrate (see figure 1A; column 5, lines 53-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the

invention was made to etch a mask in Masuoka et al. as taught by Rengarajan et al. for the purpose of creating openings.

As to claim 18, Masuoka et al. do not disclose: forming a plurality of first conductivity type implant regions in the substrate before the step of forming sidewall spacers, each of the plurality of first conductivity type implant regions formed in a respective exposed surface of the substrate.

Rengarajan et al. disclose: forming a plurality of first conductivity type implant regions ("ion implantation process") in the substrate 10 before the step of forming sidewall spacers (spacers 53), each of the plurality of first conductivity type implant regions (source and drain regions 48) formed in a respective exposed surface ("active area 24B") of the substrate (see column 9, lines 12-17). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implant a suitable p-type dopant in active areas in Masuoka et al. as taught by Rengarajan et al. for the purpose of making source and drain regions (see column 9, lines 12-17).

As to claim 20, Masuoka et al. do not disclose the predetermined depth is in the range of about 20 nm to about 500 nm.

Rengarajan et al. disclose the predetermined depth is in the range of about 20 nm to about 500 nm (less than 2000 angstroms) (see figure 1A; column 5, lines 53-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have a predetermined depth in a mask in Masuoka et al. as taught by Rengarajan et al. for the purpose of making openings with a range of depth.

As to claim 29, Masuoka et al. do not etching the substrate between the plurality of openings in the first mask to a predetermined depth before forming a plurality of first conductivity type wells over the substrate. Rengarajan et al. disclose etching (photolithographic-etching techniques) the substrate between the plurality of openings in the first mask ("masking layer 16") to a predetermined depth before forming a plurality of first conductivity type wells (openings 18 for forming active area) over the substrate (see figure 1A; column 5, lines 53-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to etch a mask in Masuoka et al. as taught by Rengarajan et al. for the purpose of creating openings.

As to claim 30, Masuoka et al. do not disclose: forming a plurality of first type implant regions in the substrate before the step of forming sidewall spacers, each of the plurality of first conductivity type implant regions formed in a respective exposed surface of the substrate.

Rengarajan et al. disclose: forming a plurality of first As to claim 18, Masuoka et al. do not disclose: forming a plurality of first conductivity type implant regions in the substrate before the step of forming sidewall spacers, each of the plurality of first conductivity type implant regions formed in a respective exposed surface of the substrate.

Rengarajan et al. disclose: forming a plurality of first conductivity type implant regions ("ion implantation process") in the substrate 10 before the step of forming sidewall spacers (spacers 53), each of the plurality of first conductivity type implant regions (source and drain regions 48) formed in a respective exposed surface ("active area 24B") of the substrate (see column 9, lines 12-17). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implant a suitable p-type dopant in active areas in

Masuoka et al. as taught by Rengarajan et al. for the purpose of making source and drain regions (see column 9, lines 12-17).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) and Rengarajan et al. (U.S. 6,323,103) and further in view of Nishida et al. (US 6,864,128).

As to claim 7, Masuoka et al. and Rengarajan et al. do not disclose the doping concentration of the first conductivity dopant is in the range of about 1.times.10.sup.17/cm.sup.3 to about 1.times.10.sup.20/cm.sup.3.

Nishida et al. (US 6,864,128) disclose the doping concentration of the first conductivity dopant (phosphorus concentration) is in the range of about 1.times.10.sup.17/cm.sup.3 to about 1.times.10.sup.20/cm.sup.3. (5x10.sup.19./cm.sup.3) (see column 8, lines 7-13; column 10, lines 6-23, lines 55-58; column 14, lines 16-21). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope the polysilicon film in Masuoka et al. and Rengarajan et al. as taught by Nishida et al. for the purpose of making gate electrodes.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413), Rengarajan et al. (U.S. 6,323,103), Nishida et al. (US 6,864,128) and further in view of Hahn (US 6,482,717).

As to claim 8, Masuoka et al. (U.S. 6,342,413), Rengarajan et al. (U.S. 6,323,103), and Nishida et al. (US 6,864,128) do not disclose a step of forming the first epitaxial layer to a larger thickness than that of the first mask to avoid epitaxial faceting; and etching back the first epitaxial layer to a smaller thickness than that of the first mask.

Hahn discloses a step of forming the first epitaxial layer (oxide layer 5) to a larger thickness (a desirable deposited thickness) than that of the first mask (layer 2) to avoid epitaxial faceting; and etching back (blanket etching) the first epitaxial layer ("oxide layer 5") to a smaller thickness than that of the first mask (layer 2) (see figures 1D-1G; column 3, lines 56-67; column 4, lines 1-37). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to selective epitaxial growth process in Masuoka et al., Rengarajan et al., and Nishida et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) and Hahn (US 6,482,717) and further in view of Nishida et al. (US 6,864,128).

As to claim 10, Masuoka et al. and Hahn do not disclose: the doping concentration of the second conductivity dopant is in the range of about 1.times.10.sup.17/cm.sup.3 to about 1.times.10.sup.20/cm.sup.3.

Nishida et al. (US 6,864,128) disclose the doping concentration of the second conductivity dopant (phosphorus concentration) is in the range of about 1.times.10.sup.17/cm.sup.3 to about 1.times.10.sup.20/cm.sup.3. (5x10.sup.19./cm.sup.3) (see column 8, lines 7-13; column 10, lines 6-23, lines 55-58; column 14, lines 16-21). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope the polysilicon film in Masuoka et al. and Hahn as taught by Nishida et al. for the purpose of making gate electrodes.

9. Claims 19, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) and Rengarajan et al. (U.S. 6,323,103) and further in view Hahn (US 6,482,717).

As to claim 19, Masuoka et al. and Rengarajan et al. do not disclose a plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process over exposed surfaces of the first conductivity type implant regions.

Hahn (US 6,482,717) discloses the plurality of first conductivity type wells (wells 6) are formed by a first selective epitaxial growth process ("selective epitaxial growth SEG"), and the plurality of second conductivity type wells (wells 6) are formed by a second selective epitaxial growth process (see abstract; figures 1D-1G; column 2, lines 60-67; column 4, lines 23-37). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include a selective epitaxial growth process in Masuoka et al. and Rengarajan et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

As to claim 23, Masuoka et al. disclose at least one of the plurality of first conductivity type wells (n type well 331-332) is a dummy first conductivity well that terminates at least one second conductivity type well (p type well 116) (see figures 2A-4D; column 9, lines 17-42).

As to claim 24, Masuoka et al. disclose at least one of the plurality of second conductivity type wells (p type well 116) is a dummy second conductivity well that terminates at least one first conductivity type well (n type well 331-332) (see figures 2A-4D; column 9, lines 17-42).

As to claim 25, Masuoka et al. disclose the first conductivity type is n-type (n-type wells 326-327) and the second conductivity type is p-type ("p type wells 324-325") (see figures 2A-2B; column 9, lines 16-47; figure 4D).

10. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) and Rengarajan et al. (U.S. 6,323,103) and further in view of Nishida et al. (US 6,864,128).

As to claim 21, Masuoka et al. and Rengarajan et al. do not disclose a doping concentration of the first conductivity type implant regions are in the range of about 1.times.10.sup.19/cm.sup.3 to about 1.times.10.sup.21/cm.sup.3.

Nishida et al. (US 6,864,128) disclose a doping concentration of the first conductivity type implant regions are in the range of about 1.times.10.sup.19/cm.sup.3 to about 1.times.10.sup.21/cm.sup.3. (5x10.sup.19./cm.sup.3) (see column 8, lines 7-13; column 10, lines 6-23, lines 55-58; column 14, lines 16-21). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope the polysilicon film in Masuoka et al. and Rengarajan as taught by Nishida et al. for the purpose of making gate electrodes.

As to claim 22, Masuoka et al. and Rengarajan et al. do not disclose the plurality of first conductivity type implant regions are formed in the substrate to a depth of about 20 nm to about 600 nm.

Nishida et al. (US 6,864,128) disclose the plurality of first conductivity type implant regions are formed in a substrate to a depth of about 20 nm to about 600 nm (thickness 10 nm of polysilicon film 16) (see column 10, lines 6-9). Therefore, it would have been obvious to a

person having ordinary skill in the art at the time the invention was made to select a range of thickness in Masuoka et al. and Rengarajan as taught by Nishida et al. for the purpose of better ion implantation.

11. Claims 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka et al. (U.S. 6,342,413) and Rengarajan et al. (U.S. 6,323,103) and further in view Hahn (US 6,482,717).

As to claim 31, Masuoka et al. (U.S. 6,342,413) and Rengarajan et al. (U.S. 6,323,103) do not disclose plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process over exposed surfaces of the first conductivity type implant regions.

Hahn (US 6,482,717) discloses the plurality of first conductivity type wells (wells 6) are formed by a first selective epitaxial growth process ("selective epitaxial growth SEG"), and the plurality of second conductivity type wells (wells 6) are formed by a second selective epitaxial growth process (see abstract; figures 1D-1G; column 2, lines 60-67; column 4, lines 23-37). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include a selective epitaxial growth process in Masuoka et al. and Rengarajan et al. as taught by Hahn for the purpose of obtaining a desirable facet formation region.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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